

CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8)

Applicant(s): Divakaruni et al.

Docket No.

BUR920000016US1

Serial No.

118850
09/718,500

Filing Date

November 22, 2000

Examiner

Samuel Gebremariam

Group Art Unit

2811

Invention: LOGIC STRUCTURE PROCESS AND APPLICATION FOR VERTICLE BIBOLAR TRANSISTOR

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Amendment Under 37 CFR 1.116

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In re patent application of

Divakaruni et al.

Serial No.: 09/718,580^{718,550}

Group Art Unit: 2811

Filed: November 22, 2000

Examiner: Gebremariam, Samuel A.

For: LOGIC STRUCTURE PROCESS AND APPLICATION FOR VERTICLE
BIPOLAR TRANSISTOR

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450AMENDMENT UNDER 37 C.F.R. §1.116

Sir:

In response to the Office Action mailed December 30, 2003, please amend the above-identified patent application as follows:

IN THE SPECIFICATION:

Please amend page 2, lines 2- 7 of the specification as follows:

It is advantageous in semiconductor manufacturing to simultaneously produce as many different types of devices on a chip ~~has as~~ possible. Such simultaneous production reduces the number of steps and the amount of material required to make the chip. This reduces the time and cost of producing semiconductor chips. Therefore, it is desirable to simultaneously form different types of transistors on a single chip.